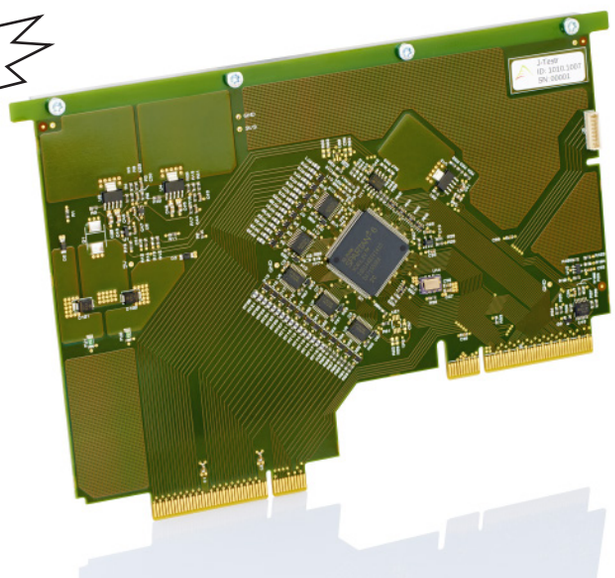
J-Testr
Completing your test solution

Information Sheet

Timer Peripheral

Technical Overview

Includes: J-SAFE TECHNOLOGY



- 32 Timer IOs (TIOs)
- 2 separate banks (16 TIOs per Bank)
- Selectable VccIO level per bank
- VccIO Voltages available to user
- 5V tolerant & protected IOs
- 5ns digital sample clock (200MHz)
- Monitor input signals up to 75 MHz
- Generate complex output signals up to 25 MHz
- Four independent advanced Signal Monitors
- Four independent advanced Signal Generators
- Flexible and simple operational modes
- 8 Generic I/O with UART & PWM features

Peripheral Details

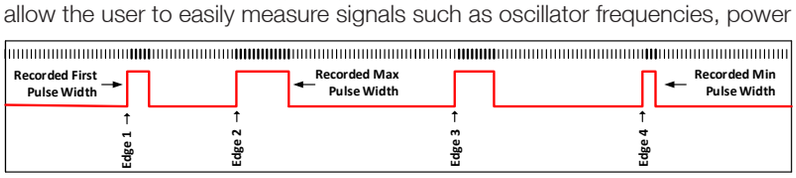
The Timer peripheral card is designed to measure and generate high speed signals using 32 Timer IO lines which are split into 2 banks of 16 lines.

Each Timer IO bank can have a separate programmable VccIO voltage level between 1.20V and 3.40V (5V input capable) to suit the requirements of the test circuits on the UUT. Both of these VccIO voltages are provided to the user at the output connector to enable the use of additional buffers on the interposer, if required.

With 'Test in Mind' all IO lines and power outputs are protected against over-voltage and over-current conditions to help avoid system damage from unexpected events.

Signal Monitors

Measurements such as frequency, duty cycle, pulse widths and pulse counts become simple, fast and easy to achieve. These features allow the user to easily measure signals such as oscillator frequencies, power supply switching frequencies, PWM signals, photodiode pulses, and countless other time critical test measurements. The high speed & flexible signal generation features allow the user to easily generate signals from simple single or multi-phase PWMs, right up to complex arbitrary digital pattern sequences.

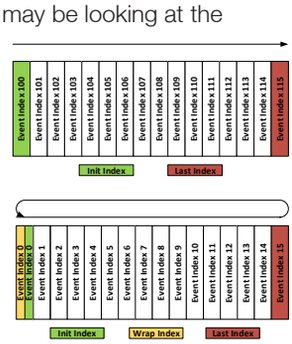


With the highly stable reference oscillator, and the frequency measurement function, the user can directly measure frequencies up to 75 MHz. Frequency measurement above this is also possible if simple frequency dividers are placed on the interposer. This allows the user to test critical on-board crystal oscillators to verify their operation, and even make sure they correct frequency value.

The Timer peripheral card's 5ns sample rate allows detection of very small pulses enabling the user to measure very fast signals. This high resolution time measurement can be used with high speed comparators on the interposer to enable the user to obtain information which would normally require a bulky & expensive external oscilloscope and inconvenient cabling. Such an example may be looking at the transient response of a PSU.

Signal Generators

The advanced signal generators allow the user to produce almost any digital pattern the user wishes using a 512 deep 'event' memory and 5ns timer resolution. Each event can control up to 16 of the Timer IOs per signal generator, and two or more generators can be used to enable all of the 32 Timer IOs to be controlled in sync. Easy to use event pointers define the initial, last and wrap-to event memory indexes. This allows multiple patterns to be stored in the event memory, and different patterns can then be 'run' simply by changing the pointers.



Signal Generator event sequences can be setup as single-shot, or allowed to run continuously until the signal generator is stopped by the user.

For further information contact your distrubutor or email: jtestr@eigerdesign.com

All specifications are subject to possible change.

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