Technical Details

J-Safe Technology Details

1 Description

The J-Safe technology is designed to have extremely fast reactions to major fault events, and upon such events, to place the motherboard and all peripheral stimulation cards into 'safe' states. When a major fault occurs a high speed 'J-Safe' hardware signal is sent to all cards within the J-Testr system to instruct them to enter a J-Safe state. The J-Safe state is the operational state all cards are put into after such a J-Safe event/trigger has occurred, e.g. after an over-voltage being detected by a power supply card. The J-Safe 'safe' state is designed to minimize the risk of damage (and/or to reduce further damage) to the UUT by removing energy transfer paths between the tester and the UUT.

Each intelligent/bus controlled J-Testr card has a dedicated J-Safe register that informs the user if a J-Safe signal is being received (RX) and/or if the card itself is generating the J-Safe signal (TX). If the card itself detected the major fault that triggered the assertion of the J-Safe signal, then the fault(s) will need to be cleared, using the appropriate fault registers for that specific card type, or via a system reset command.

The J-Safe Technology mechanism also allows the generic 'User IOs', available on every intelligent peripheral card, to be configured as external 'J-Safe' triggers. e.g. a user could add an over-voltage comparator to an additional PSU on say the interposer card, and tie into the benefits of the system wide J-Safe system.

1.1 J-Safe Register

Each J-Testr card has a register named **JSAFE_ADDR** at address 0xFE with the following bits:

Bit 0	-	JSafe_RX	-	Card is receiving a J-Safe condition
Bit 1	-	JSafe_TX	-	Card is transmitting a J-Safe condition (Generated JSafe)
Bit 2-3	-	Reserved		
Bit 4	-	UIO_GoJSafe_Event	-	UserIO Go-JSafe event triggered *(Not on motherboard)*
Bit 5-15	-	Un-used		

1.2 J-Safe 'GoJSafe'

As noted above, the J-Safe mechanism supports external triggers via 'GoJSafe' signals that can be configured from any, or all, of the 8 generic 'User IOs' available on all bus-controlled peripheral cards.

This allows the user to add their own additional customised safety circuits to the interposer, or even to use fault signals directly generated by a UUT. This means sensitive internal UUT supplies can be monitored using simple comparator circuits or POR devices, and could be used to trigger the rapid & system-wide J-Safe mechanism.

Users are also able to sense the presence of a J-Safe condition on the interposer since all 'User IOs' are set to high impedance when a J-Safe condition occurs. This could be detected and used to disconnect any external stimulation sources used within the test system, or even to provide an indicator or buzzer to alert an operator to the J-Safe condition.

Eiger Design GmbH is able to advise on circuitry for such applications.

1.3 Handling safe states

When a test program ends the user does not necessarily know the specific reason the test has failed. It could be a genuine UUT fault, or that the J-Testr has entered a J-Safe condition and shut down the UUT stimulation, causing the apparent fault to occur.

When the user's program ends it is highly recommended to follow the below procedure:

1. Check Motherboards **JSAFE_ADDR** register for the **'JSafe_RX'** bit.
2. If clear then go to end; otherwise continue
3. Check each fitted peripheral card to see if they caused the J-Safe condition to occur by checking the **JSAFE_ADDR** registers **'JSafe_TX'** bit
4. Once the peripheral card that caused the J-Safe condition is found, read the fault registers, for that card type, and report errors.
5. Clear the faults, as appropriate for that card, or issue a system reset

Note – High level driver support is provided

1.4 Latched and Unlatched States

When a J-Safe condition occurs some J-Safe states are latched, i.e. the state remains after fault cleared, and other are not latched and are only in this state until the J-Safe condition is cleared.

The reason for some unlatched states is to provide maximum protection whilst minimising complications for the user. An example is the supplies on the LV & HV IO cards being turned off during a J-Safe (as an additional measure above and beyond disconnecting the IOs) and being turned back on automatically when J-Safe is removed. The automatic turn-on saves the user having to do it, but is still 'safe' because the IOs were already latched into the disabled (Hi-Z) state.

1.5 Card Safe State and Major Fault actions

1.5.1 1000 Motherboard

1.5.1.1 Safe State

All Peripheral IOs disabled (Latched)

1.5.1.2 J-Safe Triggers

System Vin over-voltage (threshold 51V)
System Vin over-current (threshold 10.5A)
System Internal 12V over-voltage (threshold 12.6V)
System Internal 12V over- current (threshold 3.15A)
System 5V over-voltage (threshold 5.25V)
System 5V over-current (threshold 6.3A)
System 3V3 over-voltage (threshold 3.465V)
System 3V3 over-current (threshold 6.3A)
System 2V5 over-voltage (threshold 2.625V)
System 2V5 over-current (threshold 6.3A)

1.5.2 1002 JTAG IO Card

1.5.2.1 Safe State

IOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.2.2 J-Safe Triggers

None (JTAG IO card is not a Bus controlled device)

1.5.3 1004 LV Supply Card

1.5.3.1 Safe State

SupplyA Off (latched)
SupplyB Off (latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.3.2 J-Safe Triggers

Supply A High speed Over-voltage
Supply A High speed Over-current
Supply B High speed Over-voltage
Supply B High speed Over-current
External Go-JSafe

1.5.4 1005 ADC/DAC Card

1.5.4.1 Safe State

DAC Cleared using the 'nClr' hardware line (latched)
AVCC and AVSS supplies turned off (latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.4.2 J-Safe Triggers

External Go-JSafe

1.5.5 1006 Load Card

1.5.5.1 Safe State

Load A off (latched)
Load B off (latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.5.2 J-Safe Triggers

Load A Over-Power
Load B Over-Power
Load A Over-Temperature
Load B Over-Temperature
Load A Temperature Sensor Error
Load B Temperature Sensor Error
External Go-JSafe

1.5.6 1007 Timer Card

1.5.6.1 Safe State

TimerIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.6.2 J-Safe Triggers

Bank 0 Supply Over-voltage
Bank 1 Supply Over-voltage
External Go-JSafe

1.5.7 1008 HV Supply Card

1.5.7.1 Safe State

Supply A Off (latched)
Supply B Off (latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.7.2 J-Safe Triggers

Supply A High speed Over-voltage
Supply A High speed Over-current
Supply B High speed Over-voltage
Supply B High speed Over-current
External Go-JSafe

1.5.8 1009 HVIO Card

1.5.8.1 Safe State

Bank 1 Supply Off (non-latched)
Bank 2 Supply Off (non-latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.8.2 J-Safe Triggers

Bank 0 Supply Over-voltage
Bank 0 Supply Over-current
Bank 1 Supply Over-voltage
Bank 1 Supply Over-current
External Go-JSafe

1.5.9 1010 LVIO Card

1.5.9.1 Safe State

Bank 0 Supply Off (non-latched)
Bank 1 Supply Off (non-latched)
Bank 2 Supply Off (non-latched)
Bank 3 Supply Off (non-latched)
UserIOs disabled (Hi-Z) -> Achieved by clearing the IO Enable bit for this card in the motherboard register (latched)

1.5.9.2 J-Safe Triggers

Bank 0 Supply Over-voltage
Bank 1 Supply Over-voltage
Bank 2 Supply Over-voltage
Bank 3 Supply Over-voltage
External Go-JSafe