J-Testr
Completing your test solution

Information Sheet

System Overview

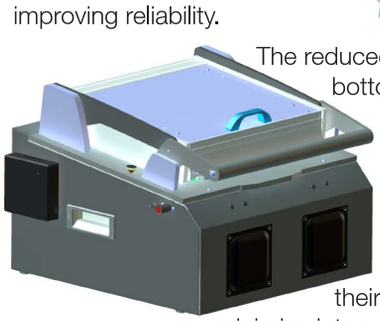
The J-Testr is a highly compact ‘all-in-one’ Ethernet and/or JTAG controlled universal & modular functional test system. The system provides a complete mechanical, power, thermal and stimulation environment to the user’s Unit Under Test (UUT). The small physical footprint and storage features make the J-Testr portable, easy to store, and maximises the use of bench space. J-Testr gives the test engineer all the features and functions needed to make a fully featured test system with ease.

Complete Test System

J-Testr's modular design and comprehensive peripheral set offers a complete test system in an easily configurable, compact unit, and allows the user to maximize test coverage of the UUT with ease. It can be controlled by an Ethernet or native JTAG interface depending on the user’s application. Using the JTAG interface, JTAG software test coverage can be significantly increased, beyond just boundary scan digital IO, to cover power rails, analogue, and bespoke functional test. J-Testr is connected to the UUT by connectors on a bespoke interface “Interposer” board, and/or flying leads, or test pins in a ‘bed of Nails’ fixture. J-Testr is reconfigurable in minutes, allowing multiple board types to be tested with one J-Testr unit. The system's communications are compatible with JTAG, conventional ATE or any socket capable software allowing the user to pick the best application for their needs. The J-Testr is ideal for companies who need a cost effective, easy-to-setup, flexible, and re-usable manufacturing test solution

Clever Mechanics

J-Testr's mechanics have been designed to be compact and easily reconfigured within minutes, thus allowing it to be used on multiple projects. Stimulation ‘peripheral’ cards plug into both the J-Testr system and the UUT ‘Interposer’ card in a swift single action. In many applications, this mechanism means that expensive and un-reliable cables between the stimulation sources and the users UUT can be completely eliminated, saving significant cost, complications, and improving reliability.



The reduced height dimensions and bottom fixings allow the J-Testr main enclosure to easily fit inside ‘Bed of Nails’ fixtures when required. The provided CAD drawings and integration examples allow users to work with their fixture supplier and thus minimise integration effort. Alternatively Eiger Design can provide a full fixture solution with J-Testr+

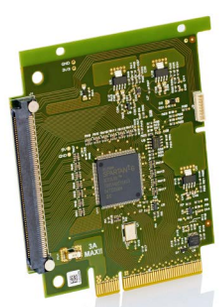
Picture: J-Testr fitted with demonstration interposer

Simple & Low-Cost Interposer

For cable-less UUT connections, signals are easily routed to the UUT using a bespoke 'interposer' card. All the nesserary drawings are provided to allow the interposer to be easily designed using standard eCAD software. The efficient auto-route features of most eCAD packages, and ever falling PCB prices, make the interposer concept simple, and cost effective to implement.

Customisable Peripheral Cards

The J-Testr system accepts up to 8 plug-in 'peripheral' stimulation cards allowing engineers to customise their test system exactly as required. All available peripheral cards have been designed with testing in mind, and they provide high performance features required to test modern UUTs.



In addition to the J-Testr’s standard suite of peripheral cards, custom peripheral cards can be achieved with the custom peripheral development kit. This allows the user to support bespoke stimulation functions that can be fully integrated to the system.

Flexible for All UUT

With both Ethernet and JTAG communication interfaces, J-Testr users can test almost any type of UUT using any type of software platform that supports either socket based or JTAG communications. So unique is the J-Testr's communications architecture, that it is able to test non-JTAG UUT’s using the same JTAG software environment as with JTAG enabled UUT designs. This flexibility allows the user to have a common test environment for all designs, saving their company cost, time, training and complexity.

Easy & Fast Programming

J-Testr programming has been designed with speed and simplicity in mind. All functions are accessed via a memory-mapped 16 bit register interface, much like those used within a microprocessor / microcontroller device, which is instantly familiar to most engineers.

This interface can be accessed via the Ethernet or JTAG communications using a very simple and logical protocol. The JTAG interface uses a very short (32-bit) JTAG data register to reduce the size loading of the JTAG chain, and allowing fast JTAG transactions. The Ethernet interface uses a very similar simple protocol, which is ASCII based, making it human-readable, and hence minimising software effort and making debugging easy.

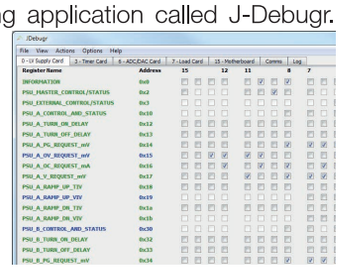
High-level Software Support

The simple communication protocol can be easily integrated into any test software environment, but Eiger Design GmbH also provides a selection of higher level drivers for popular JTAG and ATE software environments to speed-up the deployment process even further. This support includes a full set of drivers for the FREE 'Python' software development language which has become increasing popular in ATE applications.

Advanced Debugging

Debugging test applications, like all software challenges, can consume significant time and effort, often causing delays in schedules and increased costs. To assist the user in debugging their test applications, the J-Testr has a range of breakout cards which give direct access to stimulation signals. These allow the user to check & develop test routines, outside of the main test system, or even before the test system is completed.

The J-Testr also comes with a FREE 'open source' QT Windows™ software debugging application called J-Debugr. The J-Debugr software gives the user all the information about the state of the J-Testr's internal registers, as well as a full trace log of communication & registers that have been written or read. The tool is extremely similar to commercial debugger environments used for developing microprocessor applications, hence is instantly familiar to engineers.



Effective"J-Safe" UUT Protection

The "J-Safe" mechanism provides a 'high speed' protection technology designed to keep the UUT 'Safe' in cases that would normally be harmful to its circuitry. The "J-Safe" mechanism rapidly shuts down ALL possible energy sources into the UUT after a major failure (over-voltage, over-current, etc) has occured. This includes all supplies, IO, DAC, signal generators, communication lines, etc. A dedicated "Go-J-Safe" input signal is available on all peripheral cards, allowing the user to expand, if required, this powerful safety system to give ultimate UUT protection.

J-SAFE TECHNOLOGY

Picture: J-Testr with UUT mounted on top mounting plate

Key Benefits:

- Complete 'All-in-One' Test solution.
- Control via Ethernet or JTAG interfaces, with native JTAG controllable IO peripherals available.
- Super flexible, customisable, 'Bed of Nails' compatible.
- Fully integrated system power and thermal management.
- Advanced power up safety features (protects UUT).
- Very easy reconfiguration, within minutes (for re-use on multiple projects).
- One software environment to control both the 'UUT' and the 'Test Stimulus' when using a JTAG environment.
- Easy-to-use and fast programing .
- Software language independant (works with all common test software systems).
- Simple/Low-cost personalisation card ('Interposer') easily and quickly designed.
- Custom stimulation peripherals possible with 'open hardware' interface circuitry.
- Highly compact, portable, and easy to store solution.
- Cable-free connection to UUT is possible.
- Intuitive debugging tools.