J-Testr
Completing your test solution

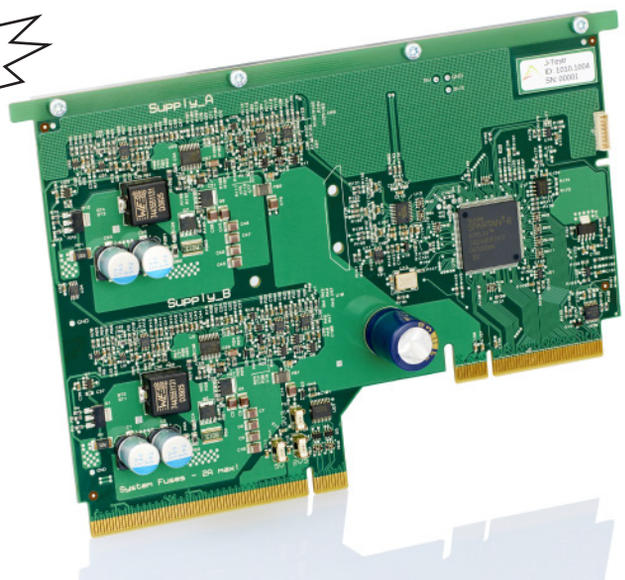
Information Sheet

# Supply Peripheral

## Technical Overview

Includes: J-SAFE TECHNOLOGY

- LV Dual 2.5V to 15V 5A supplies (1)
- HV Dual 5V to 30V 3A supplies (2)
- Programmable output with 1mV setting resolution
- Low ripple and noise
- Digitally programmable ramp up/down control
- Remote sense
- On/Off control with programmable sequencing
- Programmable independent OVP and OCP
- Latched fault reporting
- Rapid turn-off of all supplies on fault event (J-Safe)
- Programmable Power-Good indication
- Accurate/stable voltage and current monitoring
- 8 Generic I/O with UART & PWM features

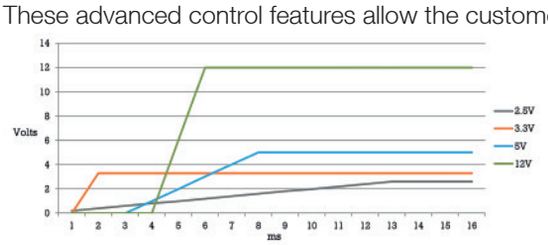



(1) 24V Input (2) 48V Input

## Peripheral Details

The supply peripheral card gives customers all the power supply features they would expect from a modern bench supply, all contained within the small footprint of a J-Testr peripheral card. In fact, with advanced features such as digitally programmable ramp rates, sequencing, and generic IO lines, these supplies offer capabilities only seen on more advanced expensive bench top supplies.

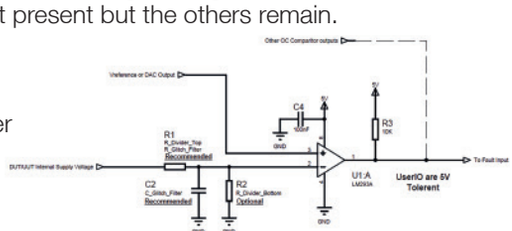
These advanced control features allow the customer to simulate complex external supply profiles, enabling testing of internal voltage monitoring chips, to prove that the UUT will function as expected under the most extreme power-up cases. The diagram, to the left, shows an example of a complex power-up profile. This is easily achieved using two J-Testr supply peripheral cards, by adjusting the ramp rate of each individual supply, and the time sequence between each supply turning on.




Accurate current and voltage monitoring/measurement is achieved using a 16 bit (noise free) ADC system. This provides the user with a measurement resolution of 1mV/1mA across the whole measurement range and high nominal accuracies of 0.125% (Voltage) and 0.25% (Current). These accurate measurements enable the user to determine if the UUT is consuming the expected current/power under different test conditions. The voltages are differentially measured at the remote sense points, hence eliminating load related voltage drops that can introduce significant power measurement errors.

As with all parts of the J-Testr system, the supply cards have been designed with test in mind, and 'J-Safe' protection features such as independent over-voltage and over-current are included. However, what is very important when functionally testing a UUT is how the power supply/supplies behave when a fault condition occurs. With the J-Testr, ALL supplies will turn off extremely rapidly during a J-Safe event, greatly reducing the risk of damage to the UUT. This is especially important if a high voltage rail is shorted to a low voltage rail, because catastrophic damage can typically occur when one supply is not present but the others remain.

Many UUTs include local 'Point of Load' regulators that can fail, producing damaging over-voltage conditions to expensive microprocessor and/or FPGAs. To help protect against these conditions, peripheral card GPIOs can be configured to provide the user a trigger input to the J-Safe mechanism. Custom user fault protection can then be easily added to the interposer using a very simple comparator circuit to trigger the same system-wide J-Safe mechanism.




All fault events are latched and can be read from registers so the user can easily track down the cause and report it to the operator.

As with all J-Testr Bus controlled peripherals, the supply card has 8 GPIO with special functions such as PWM and UARTs.

**For further information contact your distrubutor or email: jtestr@eigerdesign.com**

All specifications are subject to possible change.

**Order Number**
**LV = 8900.1010.1004**
**HV = 8900.1010.1008**