Technical Report

UUT Power up Safety

Introduction

When powering up a UUT for the first time it is never known if any faults exist that would cause the unit to become damaged. Damage to a UUT at first power up can be very costly since a lot of time and expense has already been incurred to build the product to this level. Simple process faults can cause such errors (e.g. missing/wrong component value or solder-balls or shorts). For this reason power supply protection circuits are extremely important to protect the UUT from damage on the first power-up during test.

Typically power protection comes in the form of Over-Current Protection (OCP) and Over-Voltage Protection (OVP).

Overcurrent protection (OCP)

If a UUT has as power short or other fault that causes the input current to be significantly higher than the nominal operation current, then damage can occur from the heating effect such over-currents produce. This heating effect can damage tracks and/or semiconductors. However due to thermal time constants, any damage normally occurs in a matter of milliseconds (ms) or tens of ms.

Over current circuitry must therefore react in an appropriate time to avoid damage occurring to the UUT.

Overvoltage protection (OVP):

A UUT can be presented with an over-voltage in many different ways such as an incorrectly set supply voltage, a faulty supply or even back-EMF and other inductive effects. Over-voltage conditions can cause damage in a matter of micro-seconds (us) due to the 'punch through' effect damaging the oxide layer within a semiconductor. Even if a complete failure is not caused, the oxide layer is often permanently weakened causing a high potential for early life failures.

For this reason the OVP circuits must re-act very quickly to save the UUT from damage.

Point of Load (POL) Regulators

Most modern UUT's contain at least one POL regulator to provide lower voltage supplies to FPGAs and microprocessors. Due to space restrictions, these regulators are normally very small, and do not usually contain their own over voltage protection (OVP) circuity. This means an error in these supplies could cause substantial cost damage to the UUT, especially if it is powering high end FPGA/processor devices.

Failures in such POL regulators can be caused by the below:

- Short in voltage FB loop
- Incorrect resistor values
- Supply reference error or wrongly fitted devices.

Measuring the POL output voltages provides a way to assure long term reliability, however if the OV condition is high enough the damage will be caused far quicker than a normal test measurement system will be able to react. To provide ultimate protection, particularly to expensive and hard to rework devices, these POL voltages should be monitored by a fast reacting (us range) circuit that turns the UUT input power 'off'.

Conclusion

When powering up an un-tested UUT test engineers should be aware that faults may exist that could cause significant damage. Test engineers should take appropriate steps to protect against such conditions.

Over-voltage conditions, in particular, cause significant damage very quickly. Thus OVP should always be used, especially where expensive components are at risk.

For more information on power up safety and how the J-Testr can help to protect your UUT please contact your distributor.